cronologic

TDC Modules

TimeTagger Modules
Integration Guide

www.cronologic.de

Contents

Introduction

The compact TimeTagger modules from cronologic provide a practical solution to the challenge of significantly **reducing space requirements in measurement setups and analyzers** without sacrificing performance and accuracy. They can be integrated via customer-specific analog front ends.

The **TimeTagger modules** offer the same functionality as cronologic's TimeTagger TDC cards. As such, they are ideally suitable in applications that do require a **compact form factor**, **high data-acquisition** rates, and low **multiple-hit** dead time.

This Integration Guide provides an overview of the modules operation and installation requirements. An overview of the **functionality** and the **C API** can be found in the TimeTagger4 User Guide.

This Integration Guide is also available online at docs.cronologic.de/timetaggermodule.

Module Overview

cronologic offers the TimeTagger4-10G boards as a modular version, as well, providing:

Space-saving installation
: All TimeTagger modules can be installed via board-to-board connectors with minimal hardware effort.

Integrate at minimum cost
: Our TimeTagger4 TDC modules are the perfect choice if you are looking for picosecond resolution at the best possible price/performance ratio.

Use the TiGer timing generator
: Control your device with periodic pulse patterns, the exact timing of which is measured by the TDC. You can use any input channel of our module to output these pulses.

Features

- 4-channel common-start TDC module
- Quantization (measurement resolution): 100 ps
- Double-pulse resolution: 200 ps
- Dead time between groups: none
- Minimum interval between starts: 3.2 ns
- Up to 8000 Hits per Packet
- 5 to 0.625 GHz for bursts of up to 4096 starts
- 5 to 0.625 GHits/s per channel for bursts of up to 3900 stops
- 40 MHits/s per channel of sustained stops
- 60 MHits/s over all channels of sustained stops

For an extensive overview of all features and functions, please refer to the TimeTagger4 User Guide.

1 Hardware

1.1 Overview

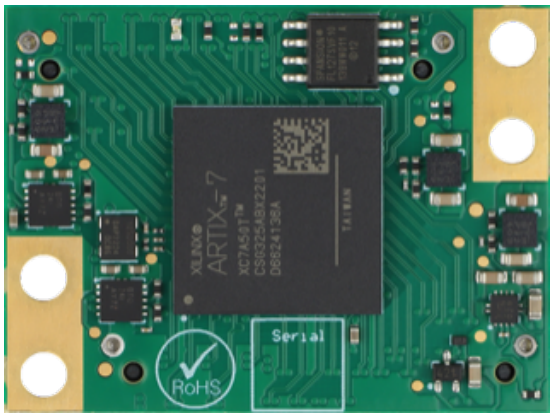

Figure 1.1: Top-view of a TimeTagger Module.

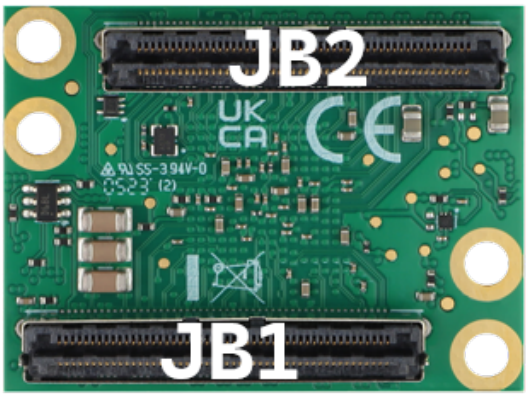

Figure 1.2: Bottom-view of a TimeTagger Module. For the pin assignment of connectors JB1 and JB2, see Section 1.5. In the above image, Pin 1 is at the bottom right of the connectors, respectively.

Figures 1.1 and 1.2 show the top and bottom view of the module.

The TimeTagger Module is connected to a carrier board using two B2B connectors Samtec Razor Beam™ LSHM-150 (JB1, JB2). Figure 1.3 shows the dimensions of the board as well as the positioning of the two B2B connectors.

Figure 1.4 shows the principle of how the TimeTagger Module may be implemented on a PCIe carrier board. Note that it only gives an overview of a possible setup. Details for the implementation are given in the sections below.

- The PCIe 12 V supply a PSU with regulated 3.3 and 2.5 V outputs supplying the TimeTagger Module with power.
- The TimeTagger Module communicates with the computer via PCIe.
- A 150 MHz oscillator is connected to the module.
- The COAX start and stop signals are discriminated and connected to the module.

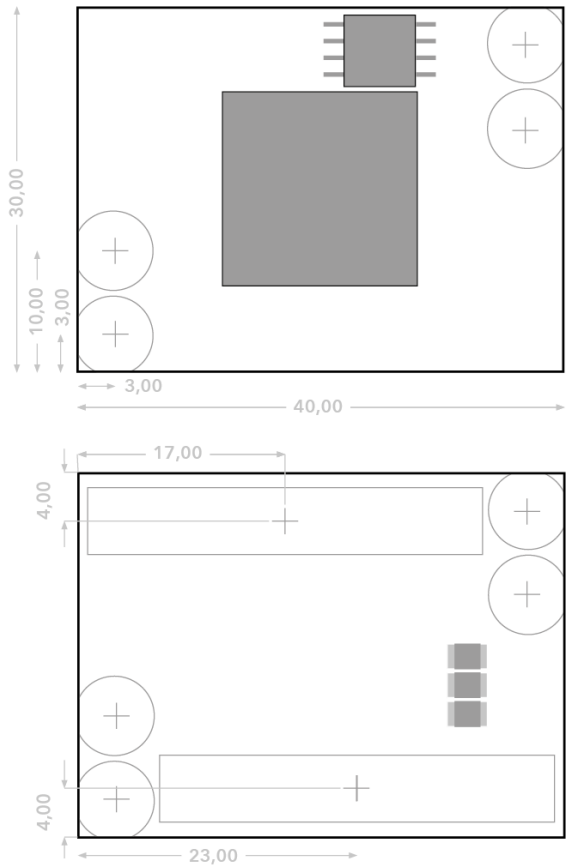

Figure 1.3: Dimensions of the module and placement of the B2B connectors and mounting holes. All dimensions are in mm. Mating height with a standard connector is 8 mm.

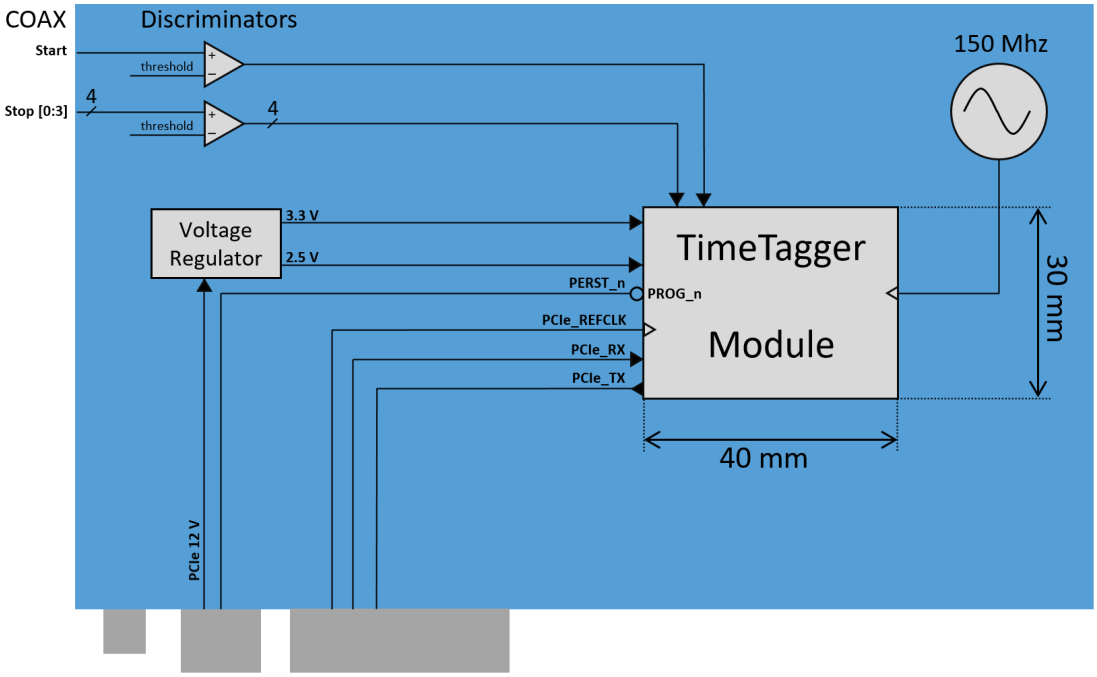

Figure 1.4: Example setup of a TimeTagger Module on a PCIe board.

1.2 Inputs and Outputs

Figure 1.5 gives an overview of the required and optional input and output signals of the TimeTagger Module. The required standards are listed in Section 1.4.

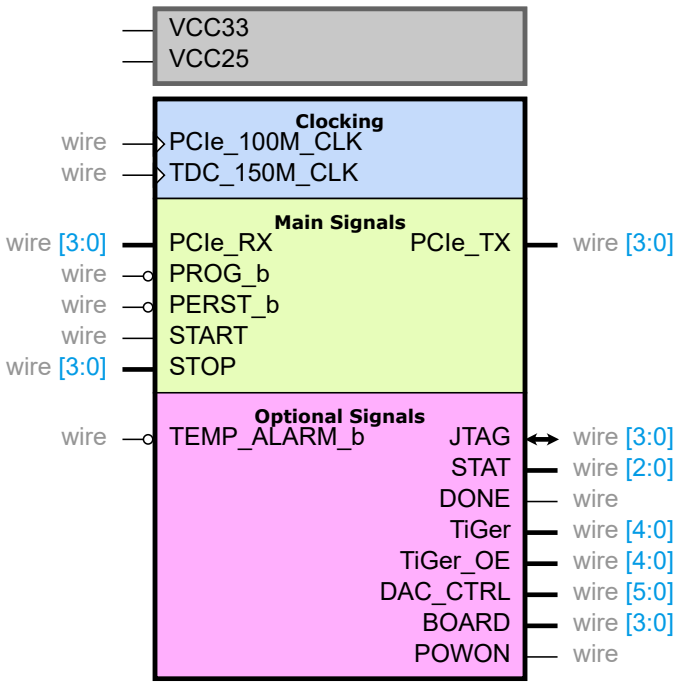

Figure 1.5: Block diagram giving an overview of the inputs and outputs of the TimeTagger Module, respectively.

1.2.1 Supply Voltages

VCC33 and VCC25

Supply voltages of 3.3 V and 2.5 V.

1.2.2 Clocking

PCIe_100M_CLK

A differential 100 MHz clock that complies with PCIe clock specifications with regard to signaling levels and jitter.

This must be synchronous to the clock of the PCIe host connected to the module. It can be taken directly from the clock of a PCIe_CEM connector.

100 nF decoupling capacitors should be placed in series of this signal to implement AC coupling.

TDC_150M_CLK

A differential LVDS clock signal with 150 MHz frequency. This can be either synchronous or asynchronous to PCIe_100M_CLK.

The quality of this clock effects the measurement accuracy of the TDC, so a low-jitter clock source must be used. Spread-spectrum clocking should be disabled for this signal.

1.2.3 Main Signals

All these signals must be correctly connected to operate the TimeTagger Module.

PROG_b

3.3 V CMOS input.

Strobe LOW to initiate a reload of the FPGA firmware.

In a PCIe-CEM system this should be connected to the PERST_b pin of the connector and provided with a 5 kΩ pull-up to 3.3 V. When connected to 3.3 V, the firmware is only loaded once at power-up.

PERST_b

3.3 V CMOS input.

Reset the PCIe core of the FPGA.

In a PCIe_CEM system, this should be connected to the corresponding signal from the edge connector. In an embedded system the requirements can vary, but it could be controlled by a microcontroller output.

Timing should comply to the PCIe_CEM specification.

PCIe_TX[3:0]

Differential PCIe output signals to transmit packets from the TimeTagger Module to the host. Compliant to PCIe standards. The _P and _N signals of each pair can be flipped to simplify routing.

The PCIe protocol will detect and correct the inversion.

Lanes 0 to 3, or lanes 0 and 1, or only lane 0 can be connected to the host. The ordering of lanes can be reversed to simplify routing.

PCIe_RX[3:0]

Same as PCIe_TX but an input for receiving packets from the host at the module. 100 nF decoupling capacitors must be placed in series to these signals.

START

Differential LVDS input to start a TDC measurement. If single ended signals or small scale signals shall be processed, a discriminator must be implemented.

This signal must not be left floating and should always be in a well-defined LOW or HIGH state.

STOP[3:0]

Differential LVDS input to create a time measurement on the respective channel.

This signal must not be left floating and should always be in a well-defined LOW or HIGH state.

1.2.4 Optional Signals

These signals are not necessary for operating the module, but they can provide useful additional features.

> **Attention:** Even if not in use, *JTAG_TCK* and *TEMP_ALARM_b* have to be connected correctly. See the descriptions of these signals for details.

JTAG signals

The JTAG port for debugging, re-flashing and interactive development of the FPGA hardware. This is usually not required for a production system, as the firmware delivered with the module provides the capability to update the firmware over PCIe.

However, we recommend implementing a JTAG connector anyway if space is available, to simplify debugging of the base board. See Figure 1.6 for the implementation.

There are various JTAG cables for FPGA development available. The following circuit is compatible to the JTAG-HS2 Programming Cable by Digilent, provided, e.g., by trenz electronic.

JTAG_TDI
: 3.3 V CMOS input.

  Data from the JTAG controller to the FPGA.

JTAG_TDO
: 3.3 V CMOS output.

  Data from the FPGA to the JTAG controller.

JTAG_TMS
: 3.3 V CMOS input.

  Control signal from the JTAG controller to the FPGA.

JTAG_TCK
: 3.3 V CMOS input.

  Clock signal from the JTAG controller to the FPGA.

  If JTAG is used, a 50 Ω termination close to the FPGA module is required.

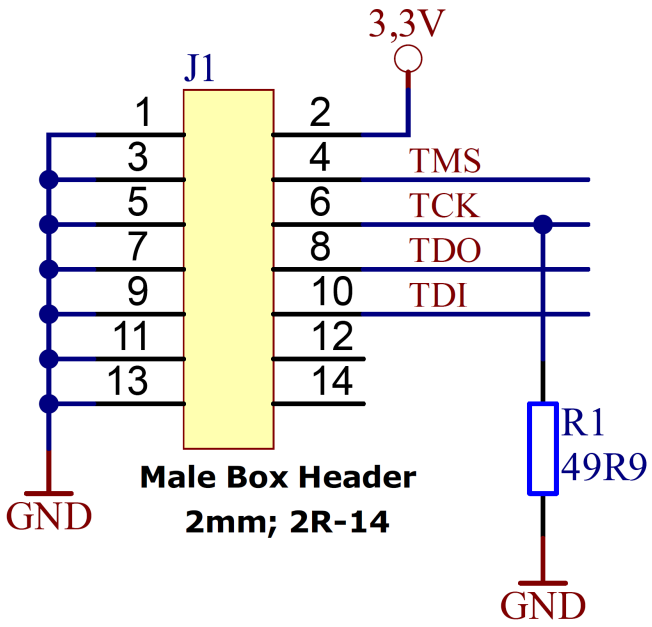

Figure 1.6: Circuit diagram for a JTAG connector.

Otherwise, if JTAG is not used, this signal must be tied to GND or 3.3 V.

Status Signals

There are four signals provided that can be used to provide information about the module status.

In the original TimeTagger4 base boards, these signals are connected to LEDs to provide visual feedback to the user. In an embedded system they could alternatively be connected to microcontroller inputs.

DONE

3.3 V CMOS output.

A high value indicates that the FPGA completed configuration. cronologic usually connects this to a red LED over a 220 Ω series resistor.

The LED is lighting up during configuration so that a failed configuration is immediately visible.

STAT_INITIALIZED

3.3 V CMOS output.

Is set to HIGH after the board is initialized by the driver.

Is reset to LOW when the device is closed by the software.

STAT_CAPTURE[1:0]

3.3 V CMOS output.

Provide status information. These can be connected to 3.3 V via 120 Ω series resistor and an LED.

STAT_CAPTURE[0] is set HIGH when the driver is in the capturing state.

Then, STAT_CAPTURE[1] becomes HIGH when a first start pulse is detected during capturing.

These bits are sticky and stay HIGH until capturing is stopped, with one exception: If missing groups are detected, STAT_CAPTURE[0] becomes LOW and STAT_CAPTURE[1] becomes HIGH.

These pins can be connected to a dual-color LED that lights up, e.g., green when capture is started, yellow when start signals are detected, and red when groups are missing. For this STAT_CAPTURE[0] should light up the green LED and STAT_CAPTURE[1] should light up the red LED.

TiGer Signals

TiGer[4:0]

3.3 V CMOS output.

These pins are controlled by the TiGer timing generator. They can be used to control the timing of the system with high precision.

TiGer_OE[4:0]

3.3 V CMOS output. Output Enable for the TiGer.

On cronologic's TimeTagger4 boards, the connectors for the TiGer outputs are shared with the TDC inputs.

To facilitate this, tri-state buffers close to the connector are used to conditionally drive the TiGer signals to the connector.

The buffers are enabled when TiGer_OE is HIGH. In an embedded system the TiGer signals usually can be routed directly to their sinks and the output enables can be left unconnected.

DAC Control

The driver for the module supports controlling of two DAC8565 digital-to-analog converters to configure the input thresholds of the discriminators and the oscillator control voltage.

In an embedded system, the same setup can be used. Alternatively, the voltages can be controlled by a microcontroller or set to fixed voltages.

DAC1 has OSC_VC on VOUTA and the discriminator threshold of the START input on VOUTD.

DAC2 has the discriminator thresholds of the for stop channels on its VOUTx outputs.

DAC3 is not supported yet. The enable is provided to allow future versions with more channels.

It is possible to change the meaning of the voltages. For example, VOUTD of DAC1 can be used as a common threshold for all inputs. But the driver will not know that and this voltage will be accessed by the user as the START channel threshold.

DAC_SYNC

3.3 V CMOS output.

Connect to the SYNC_b pins of the DACs. Avoid stubs.

DAC_SCLK

3.3 V CMOS output.

Connect to the SCLK pins of the DACs. Avoid stubs.

DAC_D

3.3 V CMOS output.

Connect to the DIN pins of the DACs. Avoid stubs.

DAC_RST_b

3.3 V CMOS output.

Connect to the RST_b pins of the DACs. Avoid stubs.

DAC_EN

3.3 V CMOS output.

Connect to the ENABLE_b pin of the DAC with the same index.

BOARD[3:0]

3.3 V CMOS output.

A bit pattern of 4 bits that is made visible in the driver API.

Can be used to communicate version or type information about the base board to the software, in case it has to act differently for certain variants.

TEMP_ALARM_b

3.3 V CMOS input.

When set to LOW, the driver will report a temperature alarm. Can be connected to the alarm output of a temperature sensor, to a microcontroller, or can be connected to 3.3 V.

POWON

3.3 V CMOS output.

This signal is set to HIGH after all power supplies of the module are stable and the FPGA on the module is configured.

It can be used to enable power supply circuits that are not required to supply the TDC module.

1.3 Routing of Differential Signals

All differential signals on the board are high speed signals that must be routed carefully to provide good signal integrity.

The routing can either be done as a coupled pair with 100 Ω differential impedance or as two independent wires with 50 Ω single ended impedance.

An uninterrupted reference plane should be on the next layer along the whole stretch of the connection. Stubs and branches must be avoided.

All differential inputs are terminated on the board with 100 Ω differential termination.

1.4 Signal Standards

The superscript next to the signal names of the tables in Sections 1.5.1 and 1.5.2 refer to the signal standard, as listed below.

[1]PCIe

Differential signals with an impedance of 100 Ω compliant with the PCIe_CEM standard.

[2]LVCMOS33

For input signals, V_{IL} and V_{IH} specify the input voltage for LOW and HIGH, respectively.

For output signals, V_{OL} and V_{OH} specify the output voltage of LOW and HIGH, respectively.

$V_{IL,min}$	$V_{IL,max}$	$V_{IH,max}$	$V_{IH,max}$	$V_{OL,max}$	$V_{OH,min}$	$I_{OL,max}$	$I_{OH,min}$
−0.3 V	0.8 V	2.0 V	3.45 V	0.4 V	2.9 V	11 mA	−11 mA

[3]LVDS

In the table below, V_{IDIFF} is the differential input voltage (U − Ū), where U is HIGH [or (Ū − U), where Ū is HIGH]. V_{ICM} is the input common-mode voltage. The input impedance is 100 Ω differential.

Symbol	Min	Typical	Max	Unit
V_{IDIFF}	100	350	600	mV
V_{ICM}	0.3	1.2	1.5	V

[4]VCC33

min. 3.2 V; max 3.4 V

[5]VCC25

min. 2.4 V; max 2.6 V

1.5 Pin Assignment

The tables in Sections 1.5.1 and 1.5.2 list the pin assignments of connectors JB1 and JB2 (see Figure 1.2).

Some signals are optional and do not have to be connected, as is described in Section 1.2.

Pins that must not be connected are marked as NC.

1.5.1 Connector JB1

Pin assignment of the JB1 connector. The superscripts refer to the signal standard (see Section 1.4)

Name	Pin	Pin	Name		Name	Pin	Pin	Name
PCIe_RX3_P[1]	1	2	*PCIe_100M_CLK_P*[1]		NC	51	52	NC
PCIe_RX3_N[1]	3	4	*PCIe_100M_CLK_N*[1]		NC	53	54	*DAC_EN2*[2]
GND	5	6	GND		NC	55	56	*DAC_RST*[2]
PCIe_RX2_P[1]	7	8	*PCIe_TX3_P*[1]		NC	57	58	*DAC_D*[2]
PCIe_RX2_N[1]	9	10	*PCIe_TX3_N*[1]		NC	59	60	*DAC_SCLK*[2]
GND	11	12	GND		Connect to JB1-83	61	62	*DAC_EN1*[2]
PCIe_RX1_P[1]	13	14	*PCIe_TX2_P*[1]		*BOARD0*[2]	63	64	*DAC_SYNC*[2]
PCIe_RX1_N[1]	15	16	*PCIe_TX2_N*[1]		*BOARD1*[2]	65	66	GND
GND	17	18	GND		*BOARD2*[2]	67	68	NC
PCIe_RX0_P[1]	19	20	*PCIe_TX1_P*[1]		*BOARD3*[2]	69	70	NC
PCIe_RX0_N[1]	21	22	*PCIe_TX1_N*[1]		NC	71	72	NC
GND	23	24	GND		NC	73	74	NC
NC	25	26	*PCIe_TX0_P*[1]		NC	75	76	NC
GND	27	28	*PCIe_TX0_N*[1]		NC	77	78	NC
GND	29	30	GND		NC	79	80	NC
GND	31	32	*TiGer2_OE*[2]		NC	81	82	*STAT_INITIALIZED*[2]
GND	33	34	*TiGer3*[2]		Connect to JB1-61	83	84	GND
NC	35	36	*TiGer2*[2]		NC	85	86	*JTAG_TDI*[2]
GND	37	38	*TiGer3_OE*[2]		NC	87	88	*JTAG_TDO*[2]
TiGer1_OE[2]	39	40	*TiGer4*[2]		NC	89	90	*JTAG_TCK*[2]
TiGer0_OE[2]	41	42	*TiGer4_OE*[2]		NC	91	92	*JTAG_TMS*[2]
TiGer1[2]	43	44	NC		NC	93	94	*PROG_b*[2]
TiGer0[2]	45	46	NC		NC	95	96	*DONE*[2]
GND	47	48	GND		*VCC33*[4]	97	98	GND
PERST_b[2]	49	50	NC		*VCC33*[4]	99	100	GND
					GND	F1	F2	GND

1.5.2 Connector JB2

Pin assignment of the JB1 connector. The superscripts refer to the signal standard (see Section 1.4)

Name	Pin	Pin	Name		Name	Pin	Pin	Name
NC	1	2	NC		*START_N*[3]	51	52	NC
NC	3	4	NC		NC	53	54	*VCC25*[5]
NC	5	6	NC		NC	55	56	*POWON*[2]
NC	7	8	NC		*STAT_CAPTURE0*[2]	57	58	*TEMP_ALARM_b*[2]
NC	9	10	*STOP3_N*[3]		*STAT_CAPTURE1*[2]	59	60	NC
NC	11	12	*STOP3_P*[3]		NC	61	62	NC
NC	13	14	*STOP2_N*[3]		GND	63	64	NC
NC	15	16	*STOP2_P*[3]		NC	65	66	NC
GND	17	18	NC		NC	67	68	NC
NC	19	20	NC		NC	69	70	NC
NC	21	22	NC		NC	71	72	GND
NC	23	24	NC		NC	73	74	NC
NC	25	26	NC		NC	75	76	NC
NC	27	28	NC		NC	77	78	NC
NC	29	30	NC		NC	79	80	NC
NC	31	32	*TDC_150M_CLK_P*[3]		NC	81	82	NC
NC	33	34	*TDC_150M_CLK_N*[3]		GND	83	84	NC
GND	35	36	GND		NC	85	86	NC
NC	37	38	NC		NC	87	88	NC
NC	39	40	NC		NC	89	90	GND
STOP1_N[3]	41	42	NC		NC	91	92	NC
STOP1_P[3]	43	44	NC		NC	93	94	NC
STOP0_N[3]	45	46	NC		NC	95	96	NC
STOP0_P[3]	47	48	NC		NC	97	98	NC
START_P[3]	49	50	NC		NC	99	100	NC
					GND	F1	F2	GND

2 Technical Data

2.1 Size and Weight

Dimensions:

30 × 40 × 5 mm

Weight:

9 g

2.2 TDC characteristics

Refer to the main TimeTagge4 User Guide.

2.3 Electrical characteristics

Symbol	Parameter	Min.	Typical	Max	Unit
P_{total}	Total power consumption		1.6	2.2	W
$VCC_{3.3}$	VCC33 voltage	3.2	3.3	3.4	V
$I_{3.3}$	VCC33 input current		470	650	mA
$VCC_{2.5}$	VCC25 voltage	2.4	2.5	2.6	V
$I_{2.5}$	VCC25 input current		10		mA

2.4 Information required by DIN EN 61010-1

2.4.1 Manufacturer

The device is a product of:

cronologic GmbH & Co. KG
Jahnstraße 49
D-60318 Frankfurt

HRA 42869 beim Amtsgericht Frankfurt/M
VAT-ID: DE235184378

2.4.2 Intended Use and System Integration

The devices are **not ready to use as delivered** by cronologic. It requires the development of **carrier boards** and **specialized software** to fulfill the application-needs of the end-user. The device is provided to system integrators to be built into measurement systems that are distributed to end users. These systems usually consist of the TimeTagger Module integrated on a PCIe carrier board, a main board, a case, application software and possibly additional electronics to attach the system to some type of detector. They might also be integrated with the detector.

The TimeTagger Module is designed to comply with **DIN EN 61326-1** when operated on a PCIe compliant main board housed in a properly shielded enclosure. When operated in a closed standard compliant enclosure, the device does not pose any hazards as defined by **EN 61010-1**.

Radiated emissions, noise immunity, and safety highly depend on the quality of the enclosure. It is the responsibility of the system integrator to ensure that the assembled system is compliant to applicable standards of the country that the system is operated in, especially with regard to user safety and electromagnetic interference.

When handling the board, adequate measures must be taken to protect the circuits against electrostatic discharge (ESD). All power supplied to the system must be turned off before installing the board

2.4.3 Recycling

cronologic is registered with the “Stiftung Elektro-Altgeräte Register” as a manufacturer of electronic systems with **Registration ID DE 77895909**.

The device belongs to **Category 9**, **“Überwachungs und Kontrollinstrumente für ausschließlich gewerbliche Nutzung.”** The last owner of the device must recycle it in compliance with

§11 and **§12** of the German ElektroG, or return it to the manufacturer’s address listed in Section 2.4.1.

3 Revision History

3.1 Firmware, Driver, and Applications

Refer to the main TimeTagger4 User Guide.

3.2 Integration Guide

1.0.1 — 2024-07-09

Rename to “Integration Guide”

1.0.0 — 2024-07-03

Initial release